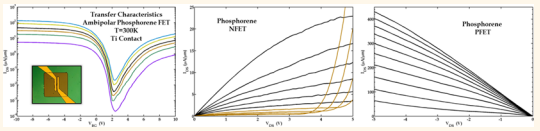
Ambipolar Phosphorene Field Effect Transistor

Saptarshi Das,*[,†,‡] Marcel Demarteau,[‡] and Andreas Roelofs[†]

[†]Center for Nanoscale Material and [‡]Division of High Energy Physics, Argonne National Laboratory, Argonne, Illinois 60439, United States

ABSTRACT In this article, we demonstrate enhanced electron and hole transport in few-layer phosphorene field effect transistors (FETs) using titanium as the source/drain contact electrode and 20 nm SiO_2 as the back gate dielectric. The field effect mobility values were extracted to be ~38 cm^2/Vs for electrons and ~172 cm^2/Vs for the holes. On the basis of our experimental data, we also comprehensively discuss how the contact resistances arising due to the Schottky barriers at the source and the drain end effect the different regime of the device characteristics and ultimately limit the ON state performance. We also propose and implement a novel technique for extracting the transport gap as well as the Schottky barrier height at the metal−phosphorene contact interface from the ambipolar transfer characteristics of the phosphorene FETs. This robust technique is applicable to any ultrathin body semiconductor which demonstrates symmetric ambipolar conduction. Finally, we demonstrate a high gain, high noise margin, chemical doping free, and fully complementary logic inverter based on ambipolar phosphorene FETs.



KEYWORDS: phosphorene · ambipolar field effect transistor · contact resistance · logic inverter

Two-dimensional layered materials are being actively investigated as an alternative to silicon for future generations of nanoelectronic devices due to their ultrathin body, which enables efficient electrostatic gate control when used in field effect transistor geometry. Pioneering work started with groundbreaking experiments regarding graphene, a monolayer of hexagonally arranged carbon atoms, by Novoselov and Geim.[1,2] Graphene has extremely high carrier mobility (~20 000 cm^2/Vs at room temperature) and the potential to reach ballistic transport at relatively large length scales; however, the absence of a finite band gap imposes severe challenges on its implementation into logic transistors which require large (at least 4 orders of magnitude) current ON/OFF ratios. A considerable effort is being dedicated to manufacturing a band gap in graphene through size quantization in nanoribbons and the electric field in bilayers.[3,4] Semiconducting transition metal dichalcogenides (TMDs), on the contrary, possess a finite and tunable band gap that can range from ~0.4 to ~2.3 eV but at the expense of low carrier mobility. Field effect transistors (FETs) fabricated on molybdenum- and tungsten-based sulfides, selenides, and tellurides have demonstrated more than 6−7 orders of magnitude current ON/OFF ratios and excellent subthreshold swings (close to an ideal value of 60 mV/decade) but with mobility values ranging from 10 to 200 cm^2/Vs.[5−15] It is important to mention here that, in the context of aggressive channel length scaling, the low mobility values of the TMDs do not invoke any concern because, for technology nodes beyond 10 nm, the transport mechanism in the semiconducting channel of the transistor will be dominated by ballistic processes instead of scattering.[16−19] However, there are many other applications like the RF transistors and thin film transistors, where high mobility is extremely desirable for high performance. Phosphorene, the youngest member (by the chronology of its discovery) of this exotic class of two-dimensional crystals, is capturing a lot of attention since in addition to a finite band gap (that can range from 0.3 eV in bulk to 1.0 eV in monolayers) it also possesses high carrier mobility of ~1000 cm^2/Vs for the hole transport.[19−23] What could potentially limit the application of phosphorene is the electron transport which so far has not been demonstrated. The availabilities of both the electrons in the conduction band and the holes in the valence band are essential features for not only complementary logic designs but also other applications. In this article, we show by tuning the work function of the contact metal and by scaling the thickness of the gate oxide that electron transport can indeed be realized in phosphorene. We report

* Address correspondence to das.sapt@gmail.com, das@anl.gov.

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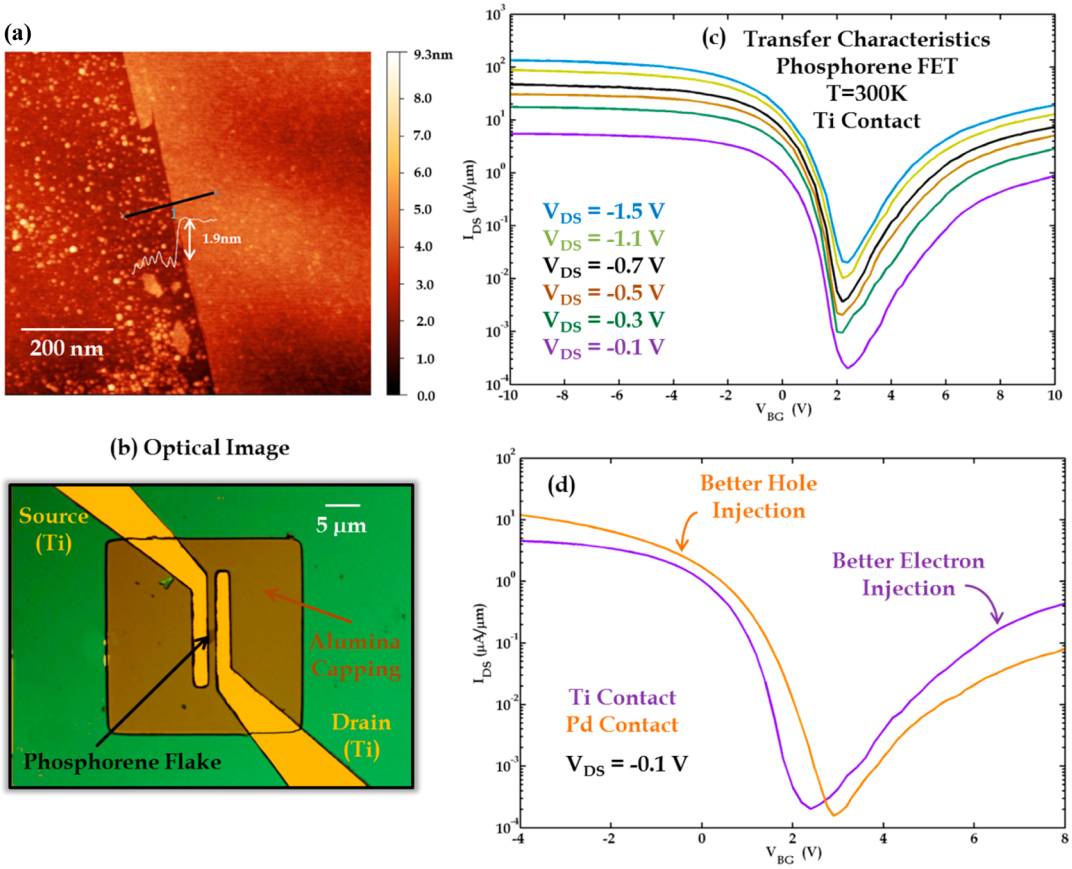

Figure 1. (a) AFM image of a 1.9 nm thick phosphorene flake with a 10 nm capping layer of alumina deposited using e-beam evaporation immediately after exfoliation in order to prevent degradation due to atmosphere. (b) Optical image of a prototype device with a 60 nm capping layer of alumina. (c) Room temperature transfer characteristics in logarithmic scale for different source to drain biases (V_{DS}) of a back-gated phosphorene FET with Ti as the source/drain contacts. (d) Transfer characteristics of phosphorene FETs with Ti and Pd contact.

record high electron field effect mobility of ~38 cm^2/Vs in phosphorene. Our hole field effect mobility of ~172 cm^2/Vs is also consistent with the earlier findings.[19−23]

One of the major concerns for high mobility transistors based on low-dimensional materials in general is the nonscalability of contact resistance. Note that in the absence of a controllable and sustainable substitutional doping scheme, one has to rely on the work function of contact metals to inject appropriate types of carriers into the respective bands of these two-dimensional semiconductors.[10,25,26] Such metal semiconductor contacts are almost always associated with finite Schottky barrier heights. The phenomenon of Fermi level pinning.[6,17,27] makes the situation even more challenging since the alignment of the metal Fermi level with the bands of the semiconducting channel is no longer determined by the work function of the contact metal. In this article, we, therefore, extract the different components of such a Schottky barrier contact resistance from our experimental device characteristics and then discuss how the different regime of device operation is affected by those. In this context, we also propose and implement a novel technique for determining the Schottky barrier height at a metal to semiconductor interface from the transfer characteristics of an ambipolar Schottky barrier field effect transistor (SBFET). This technique is further extended to determine the transport gap of the semiconducting channel material, which in our case is phosphorene. Finally, we employed electrostatic doping to combine a high-performance phosphorene p-type field effect transistor (PFET) with a phosphorene n-type field effect transistor (NFET) in a double-gated transistor geometry to demonstrate a fully complementary logic inverter. The maximum gain of our chemical doping free phosphorene inverter was found to be ~8, and the noise margin was close to its ideal value of ~2.5 V for a supply voltage of V_{DD} = 5.0 V.

RESULTS

Figure 1a shows the AFM image of a 1.9 nm thick flake with the Al_2O_3 capping layer on top. Figure 1b shows the optical image of a prototype device gated from the back. The use of 20 nm thick SiO_2 compared to conventionally used 300 nm thick SiO_2 was motivated by the fact that scaled oxide reduces the Schottky barrier tunneling distance and thereby improves the

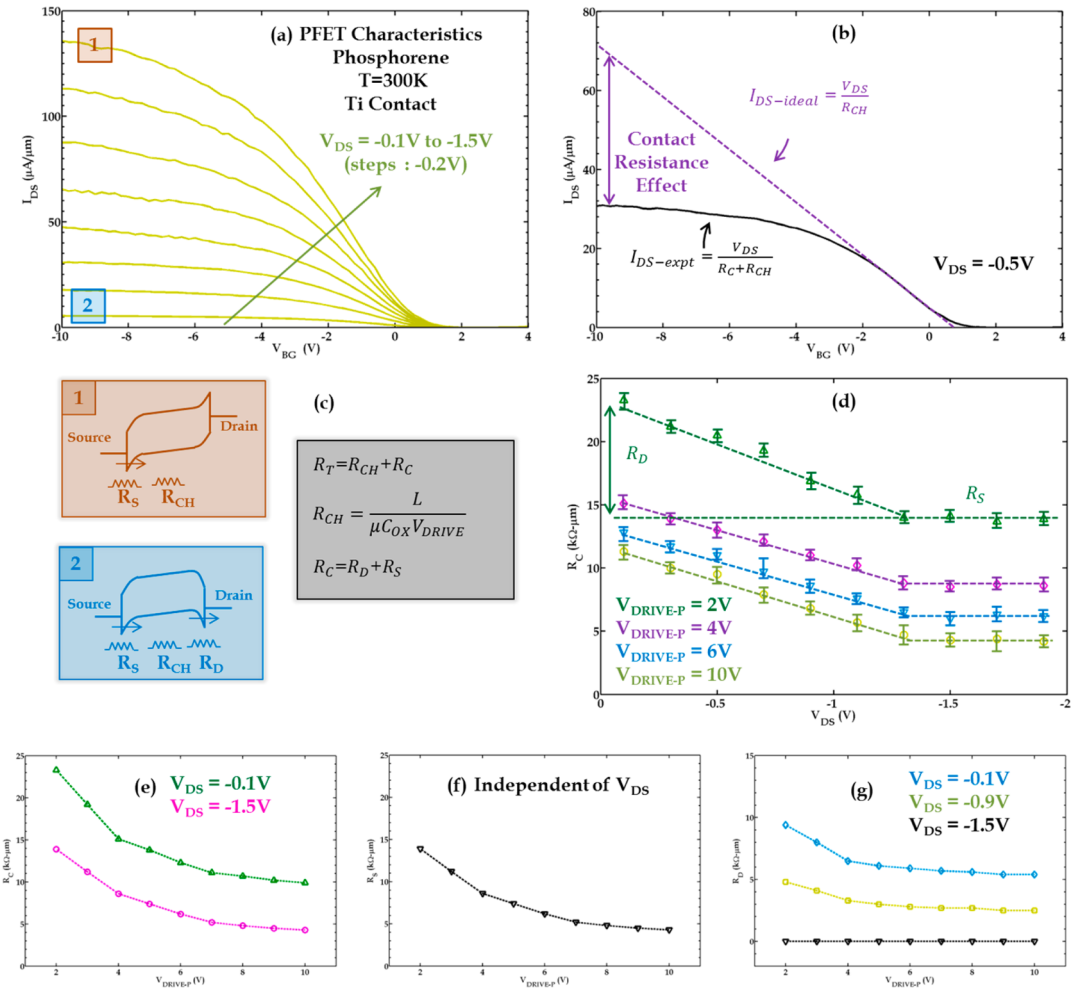

Figure 2. (a) Transfer characteristics (in linear scale) of phosphorene PFET. (b) Demonstration of the model for extracting the contact resistance (R_C) from the device characteristics. (c) Band diagrams and associated resistances for different transport regimes. (d) Different components of contact resistance extracted using panel b at different $V_{DRIVE-P}$ values and their dependence on the applied V_{DS}. The dependence of (e) R_C, (f) R_S, and (g) R_D on the back gate bias.

carrier injection.[28,29] The channel length of the device was ~2 μm. Figure 1c shows the transfer characteristics of this phosphorene FET for different negative drain biases (V_{DS}) at room temperature in logarithmic scale. Clearly, both electron and hole conduction are observed. The ON/OFF current ratios were found to be ~2.7 $\times$ 10^4 for the hole conduction and ~4.4 $\times$ 10^3 for electron conduction, which suggests that the Fermi level of Ti is aligned close to the middle of the band gap of phosphorene with a slight shift toward the valence band. Figure 1d shows the transfer characteristics of phosphorene FETs with similar flake thicknesses as Ti and Pd contacts. Both devices have a 60 nm capping layer of Al_2O_3. The fact that the Ti contact device exhibits a more pronounced electron branch compared to the Pd contact device suggests that Ti provides a smaller Schottky barrier height for electron injection into phosphorene.

Figure 2a shows the transfer characteristics of the same phosphorene FET for negative source to drain biases (V_{DS}) and negative back gate biases (V_{BG}) in linear scale. These bias conditions electrostatically dope the phosphorene with holes which results in PFET device characteristics. The field effect mobility for the hole conduction was extracted from the peak transconductance value using the conventional equation for $g_m = \mu_P C_{OX}(W/L)V_{DS}$ (where g_m is the transconductance, μ_P is the field effect mobility for the holes, and W and L are the channel width and the channel length, respectively; $C_{OX} = \varepsilon_{OX}/d_{OX}$, where ε_{OX} is the dielectric constant and d_{OX} is the thickness of the gate oxide; d_{OX} = 20 nm, and for SiO_2, $\varepsilon_{OX} = 3.5 \times 10^{-11}$ F/m, which gives $C_{OX} \sim 1.7 \times 10^{-3}$ F/m^2 and finally $L \sim 2\,\mu$m) and was found to be ~172 cm^2/Vs. It is interesting to note that the I_{DS} *versus* V_{BG} curves for any given V_{DS} saturate for large overdrive voltages ($V_{DRIVE-P} = |V_{BG} - V_{TH-P}|$, where V_{TH-P} is the threshold voltage for the hole conduction). This saturation is a result of contact resistance limiting the current flow through the phosphorene channel. In order to account for this contact resistance, we use the simple fact that the total resistance (R_T) of the phosphorene FET can be written as

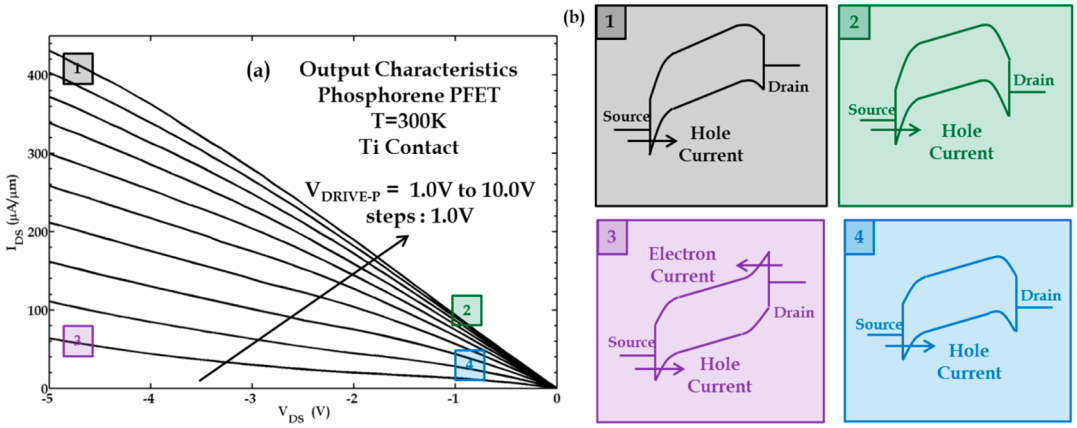

Figure 3. (a) Output characteristics and (b) associated band diagrams for different regimes of device operation for phosphorene PFET.

$R_T = R_C + R_{CH}$, where R_C is the contact resistance and R_{CH} is the channel resistance. The dependence of channel resistance on the applied back gate bias in the linear region of the device characteristics is given by $R_{CH} = L/\mu_P C_{OX} V_{DRIVE\text{-}P}$. The reader should note that the charge carrier density in the electrostatically doped phosphorene channel reaches $Q_{GATE} = 10^{13}/cm^2$ for a gate overdrive voltage of $V_{DRIVE\text{-}P} = 10$ V. At this high carrier concentration, the mobility may be impacted through scattering processes. In fact, in our earlier article,[22] we found that the carrier mobility follows a power law dependence on the carrier concentration ($\mu \propto Q_{GATE}{}^{\gamma}$) with $\gamma = -0.16$ for bilayer phosphorene. This certainly needs to be taken into account for more accurate extraction of the contact resistance. The modified equations are as follows.

$$\mu_P = \mu_{PO} V_{DRIVE\text{-}P}{}^{\gamma}$$

$$R_{CH} = \frac{1}{\mu_{PO} C_{OX} V_{DRIVE\text{-}P}{}^{1+\gamma}}$$

Note that the current and resistance values are normalized to the width. In Figure 2b, the solid black curve shows the measured current as a function of the applied back gate bias for $V_{DS} = -0.5$ V, and the dotted purple line shows the ideal case scenario without any contact resistance. Note that the dotted line is a fit to the linear portion of the I_{DS} *versus* V_{BG} curve with $V_{TH} =$ 0.7 V and $\mu_P = 172\ cm^2/Vs$. The channel resistance value was found to be 6.7 kΩ·μm for $V_{DRIVE} = 10$ V. Figure 2d shows that the extracted contact resistance decreases monotonically with the applied source to drain bias (V_{DS}) and finally plateaus at a lower value (for any given overdrive voltage $V_{DRIVE\text{-}P}$). The reader should note that the contact resistance R_C is the sum of the individual contact resistances at the source (R_S) and drain (R_D) ends due to the respective Schottky barriers, as shown in Figure 2c. For small V_{DS} in a long channel device, the channel potential at the source end is completely determined by V_{BG}, ensuring that both the height and the width of the Schottky barrier remain unchanged. The source contact resistance, therefore, remains constant as a function of the applied V_{DS}. The drain contact resistance R_D resulting from the Schottky barrier at the drain end, however, changes with the applied V_{DS} as the Schottky barrier height is monotonically reduced and finally eliminated, as shown in Figure 2c. For $V_{DRIVE\text{-}P} = 2.0$ V, R_S was found to be 13.7 kΩ·μm, and for small V_{DS} and R_S, it was found to be 9.9 kΩ·μm. This is consistent with the fact that for small V_{DS} the Schottky barriers at the source and the drain ends are almost symmetric, and therefore, the contact resistances should be very similar. The dependence of R_C, R_S, and R_D as a function of the gate bias is shown in Figure 2e−g, respectively. As expected, R_S decreases monotonically with increasing $V_{DRIVE\text{-}P}$ due to the combined effect of a reduced Schottky barrier tunneling distance and electrostatic doping of phosphorene underneath the source contact. R_D also shows a similar trend for small V_{DS} values since the Schottky barrier at the drain end influences the current conduction. The combined effect is reflected in the total contact resistance R_C. Note that similar findings have been reported for Pd and Ni contacts to phosphorene by Du *et al.*[24] using a channel length scaling study. Using the data from ref 24 and data presented in this article, the contact resistance values for Pd, Ni, and Ti contacted phosphorene are found to be 1.75, 3.15 and 4.85 kΩ·μm, respectively, for large gate bias and drain bias conditions. This is consistent with the fact that smaller work function metals give rise to larger Schottky barrier heights for the hole injection into the valence band, resulting in larger contact resistance values. The phenomenon of Fermi level pinning is present at the metal to phosphorene interface because both large work function Pd and low work function Ti contacts resulted in better hole conduction.[6,27]

Figure 3a shows the room temperature output characteristics of the phosphorene PFET for different

values of $V_{DRIVE-P}$. For large $V_{DRIVE-P}$ values, the band positions in the channel are depicted in the black and the green semitransparent boxes in Figure 3b corresponding to high and low V_{DS} values, respectively (points 1 and 2 in Figure 3a). As evident, these bias conditions are conducive for hole injection into the valence band *via* tunneling through the Schottky barrier. Electron injection into the conduction band, on the contrary, is limited due to the existence of large thermal barriers. In this context, it is important to mention that the linear nature of our I_{DS} *versus* V_{DS} characteristics should not be interpreted as the result of an Ohmic contact.[6] As comprehensively discussed in our earlier articles, the linear nature of output characteristics could be a result of either a small Schottky barrier height smeared out due to thermal broadening of the Fermi function or reduced Schottky barrier tunneling distance due to scaled oxide, scaled body thickness, or large V_{DRIVE}. In ultrathin phosphorene FETs on 20 nm SiO_2, we are, therefore, expected to observe linear I_{DS} *versus* V_{DS} characteristics. For small V_{DRIVE} values, the situation is more interesting. As the applied V_{DS} is increased, the Schottky barrier height at the drain end is reduced, and this results in a monotonic increase in the hole conduction current before it saturates, as shown in the band diagram in the blue semitransparent box in Figure 3b (point 4 in Figure 3a). The magnitude of the current in the saturation regime is controlled by the gate bias which determines the position of the bands in the channel. As the V_{DS} is increased beyond the saturation regime, the current again starts to increase because the band bending situation at the drain end becomes conducive for electrons to tunnel (through the Schottky barrier) into the conduction band, as shown in the purple semitransparent box in Figure 3b (point 3 in Figure 3a). This is another clear evidence of typical ambipolar behavior of a semiconducting channel material. Please note that in the ON state of the device characteristics, that is, above the threshold, the energy bands (Ψ_S) in the semiconducting channel of a FET do not respond in a 1:1 way to the applied gate overdrive voltage ($V_{DRIVE-P}$). This is because the channel capacitance (also referred to as the quantum capacitance C_Q) becomes significantly larger compared to the gate oxide capacitance.[30,31] In fact, it is given by the following equation:

$$d\Psi_S = \frac{C_{OX}}{C_{OX} + C_Q} dV_{DRIVE-P}$$

The threshold condition for hole conduction (for negative drain bias case) is generally reached when the valence band in the channel of the transistor aligns with the metal Fermi level at the source end. The band movement becomes increasingly slow as C_Q, which is proportional to the 2D density of states, increases monotonically for gate overdrive voltages ($V_{DRIVE-P}$) beyond the threshold.[31,32] Moreover, in the ON state of a Schottky barrier FET, most of the drain potential drops across the contacts.[30] Therefore, the slope of the valence band is similar to what has been depicted in Figure 3b. Additionally, in a long channel device (which is indeed the case for our phosphorene FETs), the gate is in firm control of the bands in the channel. All this would justify the drawing of our qualitative band diagrams and hence the explanation given for the current increase in the saturation region at low gate bias.

Figure 4a shows the transfer characteristics of the same phosphorene FET for positive source to drain biases (V_{DS}) and positive back gate biases (V_{BG}). These bias conditions electrostatically dope the phosphorene with electrons, which results in NFET device characteristics. Figure 4b shows the transconductance (g_m) for the electron transport as a function of V_{BG}. Note that the transconductance plateaus at the maximum value, which suggests that the contact resistance does not affect the electron conduction. This can also be substantiated by the fact that the channel resistance (R_{CH}) for the electron transport even for V_{DRIVE} = 10 V is ~75.4 kΩ·μm, which is much higher than the contact resistance of $R_C \sim 10$ kΩ·μm ($R_D + R_S$). The reader might question the validity of using the same contact resistance value for both electron and hole transport since the Schottky barrier height for electron and hole injection could be very different. However, as we will deduce later, the Fermi level of Ti was found to be aligned to the middle of the band gap of phosphorene, which results in similar Schottky barrier heights for electron and hole injection, and therefore, the contact resistances are indeed the same. The field effect mobility for the electron transport, extracted from the plateau in g_m, was found to be 38 cm^2/Vs. This is the highest reported electron mobility in phosphorene. Figure 4c shows the room temperature output characteristics of the phosphorene NFET for different values of V_{DRIVE}, and Figure 4d shows the associated band positions. The device characteristics corresponding to the electron transport can be explained using the exact same analogy described for the hole transport. Large V_{DRIVE} values facilitate only electron transport (the green and black semitransparent boxes in Figure 4d), while small V_{DRIVE} values coupled with large V_{DS} values enable hole tunneling current in addition to the already existing electron current (purple semitransparent box in Figure 4d). Since the hole mobility is ~5 times higher than the electron mobility, the impact is much more pronounced (as seen in the gold plots in Figure 4c) than what is observed in the output characteristics associated with the PFET.

Now we would like to justify the claim made earlier regarding the alignment of the Ti Fermi level with the energy bands of phosphorene. In this context, we report an innovative way of extracting the Schottky barrier height and the transport gap of a semiconductor from the transfer characteristics of a FET. Note that

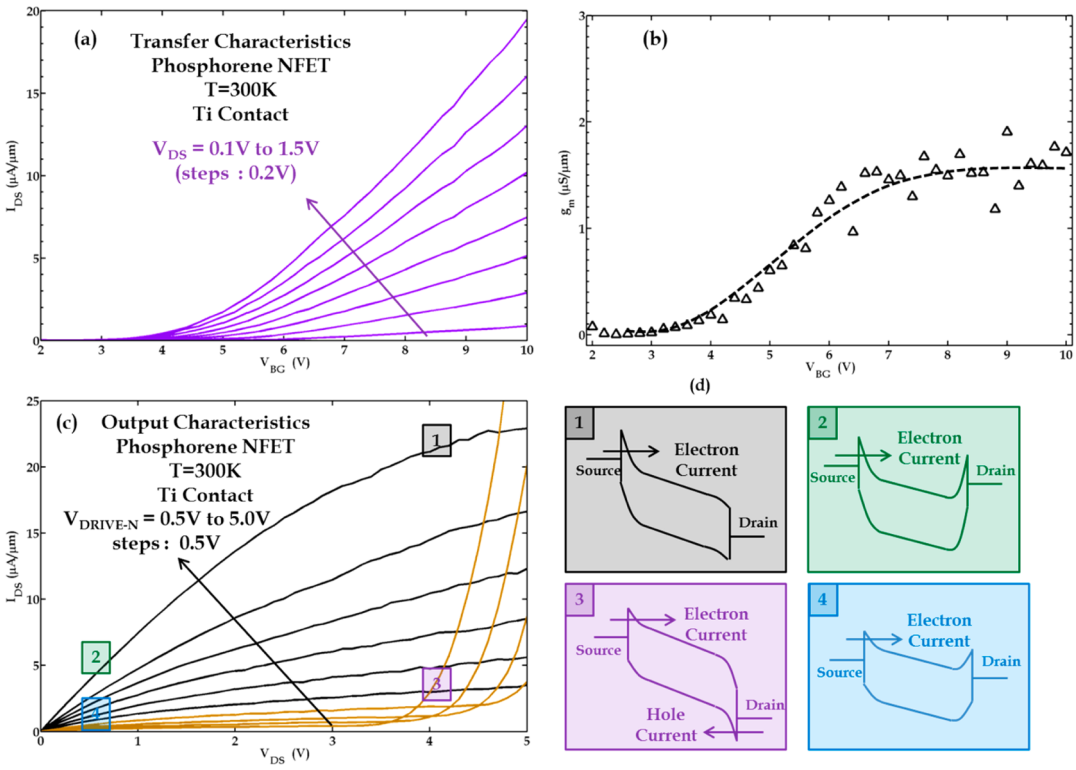

Figure 4. (a) Transfer characteristics (in linear scale) of n-type phosphorene FET. (b) Transconductance as a function of the back gate bias. (c) Output characteristics and (d) associated energy band diagrams for different transport regimes. The gold curves in panel c show how the hole conduction becomes pronounced for large drain biases for small $V_{DRIVE-N}$.

we will refer to the extracted band gap as the "transport gap" in the context of current transport. This is because the presence of surface states and unaccounted gap states can influence the current conduction in a semiconductor to a considerable extent and hence manifest in an effective band gap. Figure 5a shows the logarithmic plot of I_{DS} *versus* V_{BG} for large positive and negative drain biases. We have used V_{DS} = 1.5 V in order to determine the electron current I_N (marked by the purple semitransparent dot) and $V_{DS} = -1.5$ V in order to determine the hole current I_P (marked by the green semitransparent dot) at their corresponding threshold voltages. The threshold voltages ($V_{TH-N} = V_{BG} = 4.5$ V and $V_{TH-P} = V_{BG} = 0.5$ V) were extracted from the linear I_{DS} *versus* V_{BG} plots shown in Figures 2a and 4a. Since the magnitudes of I_P and I_N are determined by the respective Schottky barrier heights for the electron and hole injection, the ratio of I_P and I_N is a direct measure of the alignment of the metal Fermi level with the electronic bands of the phosphorene. The reader should note that for a Schottky barrier device the current at the threshold is limited by tunneling through the Schottky barrier rather than scattering in the channel due to a small number of charge carriers. Figure 5b shows the simulated ratio of hole conduction current to electron conduction current at threshold as a function of the alignment of the metal Fermi level with the middle of the band gap. For perfect mid-gap alignment, the electron and hole conduction currents must be equal with the ratio being equal to 1. The I_P/I_N ratio extracted from Figure 5a was found to be ~1.2. Note that the exponential dependence of the ratio of electron to hole current (I_N/I_P) on the relative position of the SB height (Figure 5b) makes this technique considerably robust. As seen in Figure 5c, even an order of magnitude error in the determination of I_N/I_P results in a corresponding error of 50 meV in the extraction of the SB height. So within these error bars and based on the above analysis, it is justified to assume that, for Ti contacts to phosphorene, $E_G = 2\Phi_F$.

We will now use this fact to extract the transport gap of phosphorene. If we focus on the minimum current point (I_{MIN}) of the device characteristics, we immediately realize that I_{MIN} is the superposition of two equal components: the thermionic hole emission current ($I_P = 0.5I_{MIN}$) injected from the source and the thermionic electron emission current ($I_N = 0.5I_{MIN}$) injected from the drain. Figure 5c shows the thermionic emission current calculated as a function of the barrier height using the Landauer formalism and assuming ballistic transport.[20,21] This assumption is justified since in the OFF state of the device characteristic scattering in the channel is negligible due to the absence of a sufficient number of charge carriers. In our phosphorene FETs, at the minimum current point, $I_N = I_P = 10^{-4}$ μA/μm, which corresponds to $\Phi_F = 0.43$ eV and hence $E_G = 0.86$ eV. According the photoluminescent data and DFT simulations, this band gap would

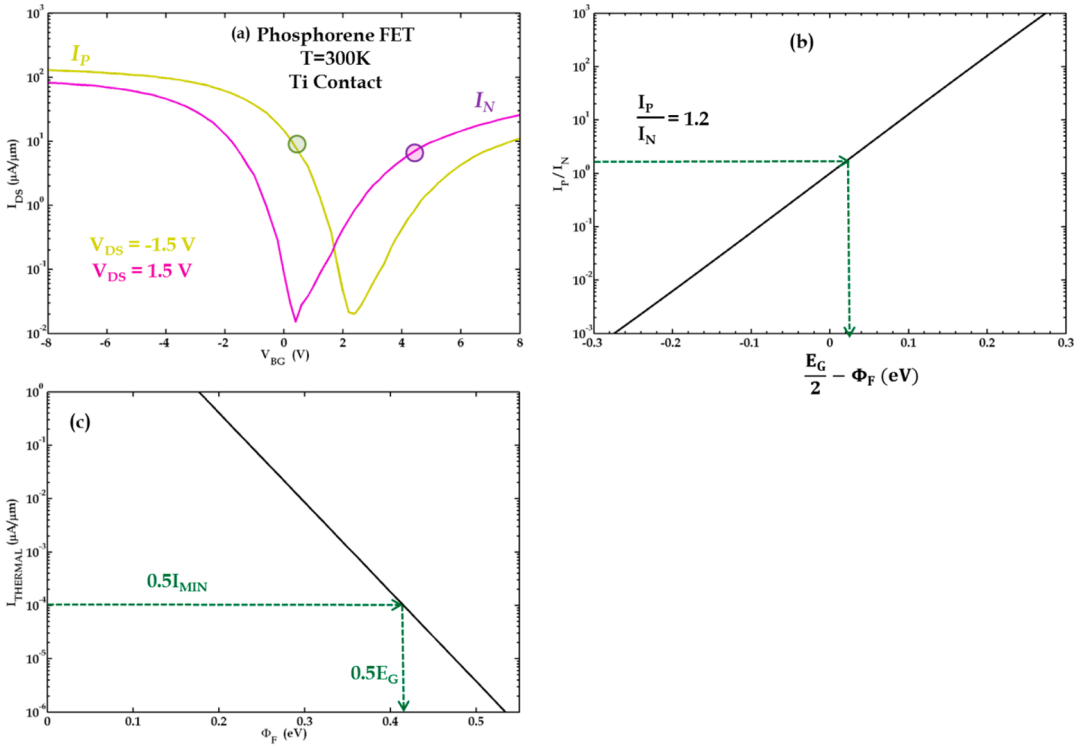

Figure 5. (a) Transfer characteristics of bilayer phosphorene FET for positive and negative V_{DS}. I_P and I_N are extracted for the same gate overdrive voltages $V_{DRIVE\text{-}N} = V_{DRIVE\text{-}P}$. (b) Simulated ratio of hole conduction current to electron conduction current for different positions of the contact Fermi level with respect to the energy bands of the phosphorene. The ratio of I_N/I_P is plotted after correcting for the different mobility values of the electron and the hole carriers. (c) Simulated thermionic current for different barrier heights.

correspond to a flake thickness in the range of 3−5 layers.[33] We would like to clarify that this innovative technique of extracting the Schottky barrier and the band gap of a semiconducting channel material can only be applied when the device characteristics are relatively symmetric (the magnitudes of I_N and I_P do not differ by more than an order of magnitude). This is indeed the case with phosphorene FETs contacted by titanium.

Finally, we demonstrate a fully complementary logic inverter based on ambipolar phosphorene FETs. Figure 6a shows the 3D cartoon projection merged on top of an optical image of a phosphorene inverter fabricated on a single flake. V_{IN} (which is equivalent to V_{BG}) is the input voltage; V_{OUT} is the output voltage, and V_{TP} and V_{TN} are the top gate voltages applied to the phosphorene flake in order to electrostatically dope it with p-type and n-type carriers, respectively. The 60 nm alumina (Al_2O_3) was used as the top gate dielectric, and Ni was used as the top gate electrode for both the PFET and the NFET. Negative top gate voltages (V_{TP}) are used to electrostatically dope the phosphorene flakes with holes, and positive top gate voltages (V_{TN}) are used to electrostatically dope the phosphorene flakes with electrons. What essentially happens is that the top gate voltage changes the position of the energy bands in the semiconducting channel, and that results in a corresponding threshold voltage shift. The shift in the threshold voltage (ΔV_{TH}) can be calculated from the principal of charge balance: $C_{TG} \cdot \Delta V = C_{BG} \cdot \Delta V_{TH}$, where C_{TG} and C_{BG} are the capacitances associated with the top and the back gates, respectively, and ΔV is the change in the top gate bias. In our experiment, $C_{TG} = 1.2 \times 10^{-3}$ F/m^2 and $C_{BG} = 1.7 \times 10^{-3}$ F/m^2, which results in a ~2.0 V shift in threshold voltage for every 3.0 V change in the V_{TP} or V_{TN}. Figure 6b shows the transfer characteristics of the PFET and the NFET as a function of the input voltage V_{IN} (V_{BG}) for $V_{TP} = -1.0$ V and $V_{TN} = 1.5$ V, respectively. Figure 6c shows the complementary inverter characteristics based on our double-gated phosphorene FET. There are three essential regions in the inverter characteristics: the region where the input voltage (V_{IN}) is relatively low, so that the output voltage (V_{OUT}) is high (shown in purple); the region where the input voltage (V_{IN}) is relatively high, so that the output voltage (V_{OUT}) is low (shown in blue); and finally, the transition region, where the input/output voltages are in an indeterminate state (an ambiguous region between high and low shown in green). The transition region is defined as the region where the gain (G) of the inverter is more than 1. Note that the gain (G) is the slope of the inverter characteristics; that is, $G = dV_{OUT}/dV_{IN}$. An ideal inverter should have infinite gain, which eliminates the transition region. Figure 6d shows the gain of our fully complementary bilayer phosphorene inverter as function on V_{IN}. The maximum gain was found to be 8.

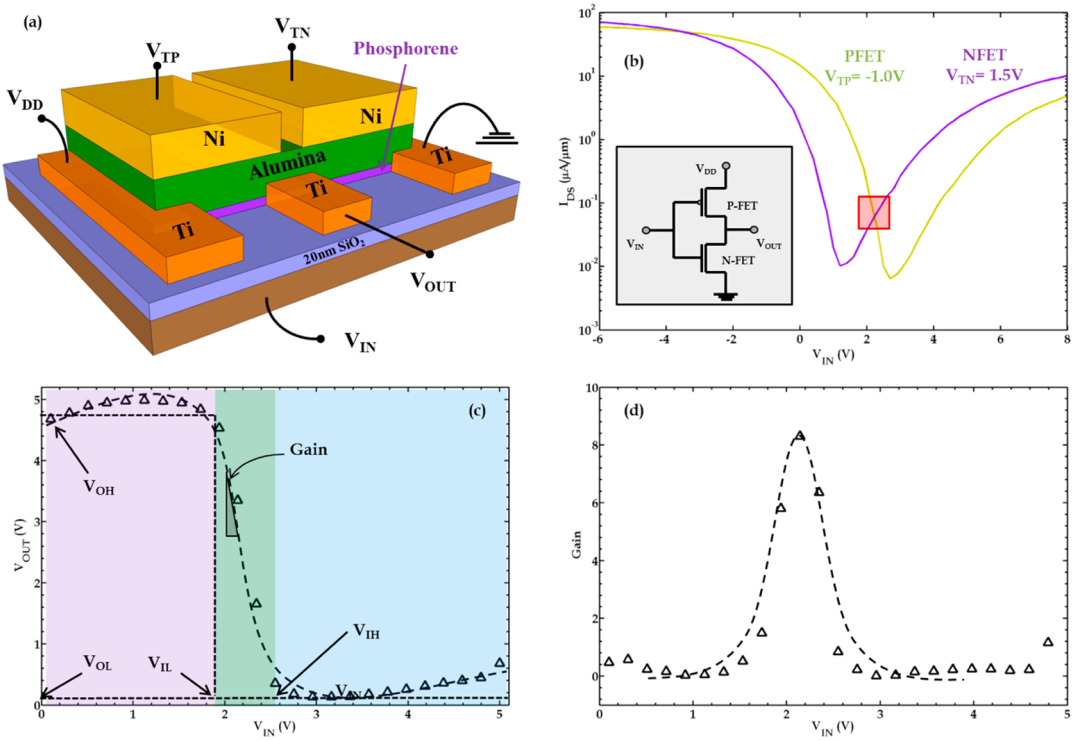

Figure 6. (a) Three-dimensional cartoon of a double-gated phosphorene FET structure used for the logic inverter. (b) Transfer characteristics of phosphorene PFET and phosphorene NFET realized through electrostatic doping. (c) Transfer characteristics of phosphorene logic inverter. (d) Gain of the inverter as a function of the input voltage.

The gain of the inverter is the highest when the intersection of the PFET and NFET transfer characteristics occurs in the steepest portion of their subthreshold behavior. This is very obvious since a steeper subthreshold swing signifies rapid changes in the corresponding current levels and hence abrupt transition from the PFET to the NFET and *vice versa*. The low gain in our inverter, therefore, can be explained from the fact that the subthreshold slopes of our PFET and NFET at the cross-over point (marked by the red box in Figure 6b) are ~0.6 V/decade, which is 10 times worse than the ideal achievable slope of 60 mV/decade.

Noise margin (NM) is another important parameter in the context of the inverter which determines how stable the output is with respect to signal interference at the input. As shown in Figure 6c, the input voltage is considered to be at logic high ("1") if $V_{IN} > V_{IH}$ and at logic low ("0") if $V_{IN} < V_{IL}$. This is because input voltages in these ranges can produce unambiguous output logic levels. V_{OH} and V_{OL} are, respectively, the ideal logic high and logic low of the inverter. Noise margins for high input (NM_H) and noise margins for low input (NM_L) are, therefore, defined as $NM_H = V_{OH} - V_{IH}$ and $NM_L = V_{IL} - V_{OL}$. For a supply voltage of $V_{DD} = 5.0$ V, we obtained a nearly ideal noise margin of ~2.25 V for the high input and 1.85 V for the low input. We would like to remind the reader that the inverter characteristics could be strongly impacted if there is hysteresis in the device characteristics. Our back-gated phosphorene devices show a hysteresis of ~200 meV, which is considerably low and does not influence the inverter operation (see Supporting Information).

CONCLUSION

In conclusion, we have successfully demonstrated an ambipolar phosphorene field effect transistor with record high electron mobility. We also extracted the contact resistance values in our Schottky barrier phosphorene FETs and comprehensively discussed its effects on the device performance. We proposed and implemented a novel technique of extracting the Schottky barrier height and the transport gap of an ultrathin body semiconductor like phosphorene from the field effect characteristics of a transistor. Finally, we demonstrate a fully complementary inverter based on ambipolar phosphorene FETs.

METHODS

Phosphorene flakes obtained from smart elements (http://www.smart-elements.com/) were mechanically exfoliated on 20 nm thick SiO_2 layers on highly doped Si substrates used as the back gate. The use of 20 nm thick SiO_2 compared to conventionally used 300 nm thick SiO_2 was motivated by the fact that scaled oxide reduces the Schottky barrier tunneling distance and thereby improves the carrier injection.[28,29] Since thin phosphorene layers are highly unstable in air, immediately

after the exfoliation, the substrate was transferred into a high vacuum electron-beam evaporator to deposit a 10 nm thick layer of alumina (Al_2O_3). Note that the presence of a transparent Al_2O_3 film does not prevent optical identification of thin flakes under the microscope. Figure 1a shows the AFM image of a 1.9 nm thick flake with the Al_2O_3 coating on top. Next electron-beam lithography was used to pattern the source/drain contact electrodes. Right before the metal deposition, the Al_2O_3 layer was removed from the contact area by submerging the sample in MF26A developer for 20 s, which does not react with phosphorene (see Supporting Information). The 70 nm thick titanium was used as the contact metal. Use of low work function metal such as Ti compared to high work function metals such as Ni, Au, or Pd reduces the Schottky barrier height for electron injection and thereby facilitates electron transport. Finally, atomic layer deposition (ALD) was used to deposit an additional 50 nm thick Al_2O_3 film on top of the existing 10 nm Al_2O_3. The ALD was performed at 240 °C using alternating exposures of trimethylaluminum $Al(CH_3)_3$ and H_2O. The presence of a 10 nm buffer layer of Al_2O_3 prevents the reaction of water with phosphorene during the initial growth cycles of Al_2O_3. The total capping layer thickness was 60 nm.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: More information on the effect of MF26A developer on phosphorene flakes and hysteresis in the phosphorene devices is provided. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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